REMARKS

The applicant has carefully considered the Office action dated July 21, 2005 and the references it cites. By way of this Response, claims 1,2, 6, 11, and 12-16 have been amended, claims 18-24 have been cancelled without prejudice to their further prosecution, and new claim 25 has been added. In view of the following, it is respectfully submitted that all pending claims are in condition for allowance and favorable reconsideration is respectfully requested.

As an initial matter, applicant notes that the dependency of claim 16 has been amended as suggested by the Examiner to correct the antecedent basis issue. It was originally intended that claim 16 depend on claim 15. The Examiner is thanked for detecting this typographical error.

Turning to the art rejections, the Office action rejected all pending claims as being unpatentable over one or more of Miller et al., U.S. Patent 6,759,687, Tomita et al., U.S. Patent 5,666,008, and Reedy et al., U.S. Patent 6,583,445. The applicant respectfully traverses these rejections.

By way of background, and as explained in the background section of the instant application:

> **[0002]** Optical flip chip packages often include a substrate, a waveguide mounted on the substrate, and a flip chip optically coupled to the waveguide. To achieve acceptable optical coupling between the optical flip chip die and the optical waveguide, it is important to control the distance between the flip chip die and the substrate. If the distance between the flip chip die and the substrate is too large, the optical coupling between the optical waveguide and the optical flip chip die may be poor, due to optical signal divergence. If the distance between the flip chip die and the substrate is too small, the

> optical waveguide and/or the optical flip chip die may be damaged during bonding of the chip to the substrate.
>
> **[0003]** Known methods of maintaining separation distance between the optical flip chip die and the substrate include using large solder balls on the optical flip chip die. As optical flip chip packages exhibit increasingly finer pitch and higher optical I/O (input/output) density, solder bridging (e.g., electrical shorts created in the soldering process when the solder melts and inadvertently connects adjacent electrical contacts) has become a serious problem. Increasing the amount of solder between the flip chip and the substrate increases the likelihood of solder bridging. ***Therefore, using large solder balls to achieve a desired separation between the optical flip chip die and the substrate during the bonding process, increases the likelihood of solder bridging.***

(emphasis added)

Independent claim 1 recites a method which overcomes the problems associated with large solder balls by coupling at least one spacer having a melting point above solder to the chip die or the substrate, and by bonding the chip die to the substrate without melting the spacer such that the length of the spacer substantially defines the distance between the chip die and the substrate. None of the cited art teaches or suggests such a method.

For example, Miller et al. expressly follow the prior art solder ball approach described in paragraphs **[0002]** and **[0003]** of the applicant's specification. In particular, Miller et al. use "solder bump reflow technology" to couple an optoelectronic device to an optical device system. (See, Miller at Col. 4, lines 44-48). Miller et al. do ***not*** employ a spacer having a melting point above solder to control the distance between the optoelectronic device and the optical device system. On the contrary, Miller et al. indicate:

> In addition, optical lenses 60, 62 and optical device 44 are aligned along Z-axis 68 [i.e., vertically] to achieve a desired focal distance between the optical device 44 and optical element 52. In the embodiment of FIG. 2, ***the Z-axis alignment is achieved*** by adjusting the dimension 70 of solder bumps 66 along Z-axis 68. Dimension 70 may be ***controlled by balancing surface tension and gravitational forces at the bonding temperature based upon a number of parameters, including individual solder bump volumes, wettable pad sizes, substrate mass and solder surface tension***.

(Miller, Col. 5, lines 35-44)(emphasis added). In view of the foregoing, it is quite evident that Miller does not contemplate, teach or suggest employing a spacer as recited in claim 1. Accordingly, absent hindsight reference to the applicant's disclosure, it is clear that the rejections based solely on Miller et al. must be withdrawn.

The other cited references do not overcome the deficiencies of Miller et al. For instance, Tomita et al. also fails to teach or suggest a spacer as recited in claim 1. Tomita et al. couples a chip 1 to a substrate 7 with connecting terminals 5 and a "plurality of thin, very flat connecting patterns 6 formed on the upper surface of the ..." substrate 7. (Tomita et al., Col. 5, lines 27-32). The thin, very flat patterns 6 are connecting pads which may be made of copper of the like (Tomita et al., Col. 5, lines 61-63). The connecting terminals 5, which account for the vast majority of the vertical space between the chip 1 and the substrate 7, are large solder balls, just as in Miller et al. (See, Col. 5, lines 59-61). As such, absent improper hindsight reference to the applicant's disclosure, a person of ordinary skill in the art would not find a spacer such as recited in claim 1 in Tomita et al.

Given the fact that both Miller et al and Tomita et al. employ large solder balls and no spacer, the combination of Tomita et al. and Miller et al. would likewise employ such large solder balls and no spacer. As discussed above, this is merely the state of the prior art discussed in the background section of the applicant's specification. As such, the combination of Miller et al and Tomita et al. does not teach or suggest the recitations of claim 1.

Reedy does not appear to overcome the deficiencies of Miller et al. and Tomita et al. Like those references, Reedy employs a large solder ball 18. Accordingly, irrespective of how one combines Miller et al., Tomita et al., and Reedy et al., one does not arrive at the method recited in claim 1. Accordingly, it is respectfully submitted that claim 1 and all claims depending therefrom are in condition for allowance.

Independent claim 12 is also allowable. Claim 12 recites a method comprising: coupling at least one spacer to a first one of the substrate or the flip chip die; and bonding the at least one spacer to the at least one conductive pad on the second one of the optical flip chip die or the substrate by melting the conductive pad and without melting the spacer, such that the spacer retains its length during and after bonding. As discussed in detail above, none of Miller et al., Tomita et al., and/or Reedy et al., whether taken alone or in combination, teach or suggest such a method. Accordingly, claim 12 and all claims depending therefrom are in condition for allowance.

In view of the foregoing, it is respectfully submitted that all pending claims are in condition for allowance.

Before closing, the applicant notes that the amendments to the dependent claims are not necessary for patentability as demonstrated by the

fact that the dependent claims depend directly or indirectly from an allowable independent claim, and the amendments to the dependent claims were not argued herein as a basis for patentability. Consequently, the above-noted amendments do not give rise to prosecution history estoppel or limit the scope of equivalents of the claims under the doctrine of equivalents.

If the Examiner is of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is invited to contact the undersigned at the number identified below.

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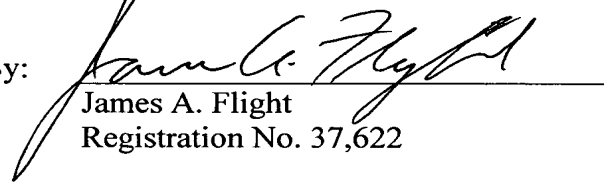
By: 
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